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| **Name of the Faculty : Sh. Krishan Lal** | | | |
| **Discipline : Computer Engg.** | | | |
| **Semester : IIIrd** | | | |
| **Subject : DIGITAL ELECTRONICS** | | | |
| **Lesson Plan Duration : Sep.-2023** | | | |
| **Work Load (Lecture/ Practical) per week (in hours): 03 HOURS (Lecture)** | | | |
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| **Week** | **Theory** | | **Practical** |
| **Lecture day** | **Topic (including assignment/ test)** | **Topic** |
| **1st** | **1** | Introduction about subject. | Introduction about instruments to be used in practical work. |
| **2** | Distinction between analog and digital signal. Applications and advantages of digital signals. |
| **3** | Binary, octal and hexadecimal number system. |
| **2nd** | **4** | Conversion from decimal and hexadecimal to binary and vice-versa. | Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates |
| **5** | Binary addition and subtraction including binary points. 1’s and 2’s complement method of addition/subtraction. |
| **6** | Concept of code, weighted and non-weighted codes, examples of 8421, BCD, excess-3 and Gray code. |
| **3rd** | **7** | Concept of parity, single and double parity and error detection | Realisation of logic functions with the help of NAND or NOR gates |
| **8** | Concept of negative and positive logic |
| **9** | Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates |
| **4th** | **10** | NAND and NOR as universal gates. | To design a half adder and full adder using XOR and NAND gates and verification of its  operation. |
| **11** | Introduction to TTL and CMOS logic families |
| **12** | Postulates of Boolean algebra, De Morgan’s Theorems. |
| **5th** | **13** | Implementation of Boolean (logic) equation with gates | To design a half adder and full adder using XOR and NAND gates and verification of its  operation. |
| **14** | Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits |
| **15** | Half adder and Full adder circuit, design and implementation. |
| **6th** | **16** | 4 bit adder circuit | Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops). |
| **17** | Four bit decoder circuits for 7 segment display and decoder/driver ICs. |
| **18** | Basic functions and block diagram of MUX and DEMUX with different ICs |
| **7th** | **19** | Basic functions and block diagram of Encoder | Verification of truth table for encoder and decoder ICs. |
| **20** | Concept and types of latch with their working and applications |
| **21** | Operation using waveforms and truth tables of RS, T, D F/F. |
| **8th** | **22** | Master/Slave JK flip flops. Race around condition. | Verification of truth table for Mux and DeMux |
| **23** | Difference between a latch and a flip flop |
| **24** | Introduction to Asynchronous counters. |
| **9th** | **25** | Introduction to synchronous counters. | To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation. |
| **26** | Binary counters |
| **27** | Divide by N ripple counters |
| **10th** | **28** | Decade counter, Ring counter | To design a 4 bit ring counter and verify its operation. |
| **29** | Introduction and basic concepts including shift left and shift right. |
| **30** | Serial in parallel out, serial in serial out shift register. |
| **11th** | **31** | Parallel in serial out, parallel in parallel out shift register. | Use of Asynchronous Counter ICs (7490 or 7493) |
| **32** | Universal shift register |
| **33** | Working principle of A/D converters |
| **12th** | **34** | Brief idea about different techniques of A/D conversion and study of : Stair step Ramp A/D converter | To design and verify ADC |
| **35** | Dual Slope A/D converter |
| **36** | Successive Approximation A/D Converter |
| **13th** | **37** | Working principle of D/A converters | To design and verify DAC |
| **38** | Binary Weighted D/A converter |
| **39** | R/2R ladder D/A converter |
| **14th** | **40** | Applications of A/D and D/A converter. | To design and verify ALU 74181 |
| **41** | Memory organization, classification of semiconductor memories |
| **42** | RAM, ROM, PROM, EPROM, EEPROM, static and dynamic RAM |
| **15th** | **43** | introduction to 74181 ALU IC | Internal Viva of all Practical. |
| **44** | Revision |
| **45** | Revision |
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